Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **N. Q**
2. **N/C**
3. **A1**
4. **A2**
5. **B**
6. **Q**
7. **GND**
8. **N/C**
9. **RINT**
10. **CEXT**
11. **REXT/CEXT**
12. **N/C**
13. **N/C**
14. **VCC**

**.050"**

**.060”**

**14 11 10**

**9**

**7**

**3 4 5 6**

**3**

**121A**

**MASK**

**REF**

**Top Material: Si**

**Backside Material: Al**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: 121A**

**APPROVED BY: DK DIE SIZE .050” X .060” DATE: 6/13/22**

**MFG: TEXAS INSTRUMENTS THICKNESS .016” P/N: 54121**

**DG 10.1.2**

#### Rev B, 7/19/02